IN THE SPECIFICATION:

Please amend the paragraph beginning at page 1, line 10 as follows:

Dielectric material is used to isolate metal lines in the multilevel interconnects process to prevent ~~the~~ shorts from occurring between two metal lines. Dielectric material used between two layers of metal lines is called intermetal dielectric (IMD). Because the surface of wafer is rugged after metal lines are formed thereon, the dielectric material subsequently deposited is also rugged. Therefore, the flatness of the IMD is the determining factor for the patterning of vias therein and metal wires thereon.

Please amend the paragraph beginning at page 1, line 17 as follows:

The planarization process is the key step for ensuring that high-density lithography can be performed, because light scattering problems can only be avoided in exposure steps when an IMD with sufficient flatness is provided. Therefore, when the IMD is sufficiently flat, a precise pattern-transferring step can be performed. Chemical mechanical polishing (CMP) is the technique that provides global planarization in current semiconductor processing. The CMP technique involves using a reagent to form a chemically altered layer on the non-planar surface of the material to be polished, followed by a mechanical removal of the chemical altered layer from the underlying bulk material.

Please amend the paragraph beginning at page 1, line 26 as follows:

The polishing slurry or the reagent used in a CMP process consists of a solvent and abrasive particles dispersed in the solvent. The solvent of the slurry chemically

PAGE 5/14 * RCVD AT 4/28/2004 10:13:02 AM [Eastern Daylight Time] * SVR:USPTO-EFXRF-1/4 * DNIS:8729306 * CSID:248 433 7274 * DURATION (mm-ss):03-50

depletes, loosens, or modifies the composition of the material to be removed. The highly abrasive particles in the slurry, in combination with the rotating polishing pad, then physically remove the chemically modified unwanted material and polish the underlying surface. Since the abrasive particles in the polishing slurry are structurally very hard, scratches are easily induced on the surface of some materials during the CMP process. The problem of bridging is then likely to occur in the subsequent process, which affects the reliability of the device. ~~Besides, a~~ A wet cleaning step is additionally needed to remove the abrasive particles used during the CMP.

Please amend the paragraph beginning at page 2, line 10 as follows:

The present invention provides a planarization method using anisotropic wet etching. According to one preferred embodiment of this invention, this method can be applied to planarize an insulating layer with an uneven surface on a substrate. H_2SO_4, H_3PO_4, HF and H_2) are mixed to form an etching solution. The substrate is placed into the etching solution to make the etching solution pass the surface of the insulating layer at a flow rate to etch the insulating layer. After a period of etching time, the insulating layer with a more planar surface can be obtained.

Please amend the paragraph beginning at page 3, line 11 as follows:

This invention ~~utilize~~ utilizes an etching solution having different flow rate on ~~an~~ a thin film having ~~an~~ a rugged surface to etch the protrusions at a larger etching rate then the recess. Hence, the rugged surface of the thin film is planarized.

PAGE 6/14 * RCVD AT 4/28/2004 10:13:02 AM [Eastern Daylight Time] * SVR:USPTO-EFXRF-1/4 * DNIS:8729306 * CSID:248 433 7274 * DURATION (mm-ss):03-50

Please amend the paragraph beginning at page 5, line 1 as follows:

In Fig. 2B, after a period of time of etching, the insulating layer 220 is transformed to the insulating layer 220a. The level difference between the top surface and bottom surface of the insulating layer 220 is h, and h is much smaller than H. Therefore, the planarity of the insulating layer 220a is much better than the insulating layer 220. In the etching reaction, the etching rate is determined by the arrival rate of the etchant molecules to the surface being etched. Consequently, the flow rate of the etching solution is approximately proportional to the etching rate. The flow rate V1 of the etching solution near the surface of the insulating layer 220 is slower, and the etching rate of the bottom surface is slower. The flow rate V2 of the etching solution at a distance from the surface of the insulating layer 220 is faster, and the etching rate of the top surface is faster.

Please amend the paragraph beginning at page 5, line 13 as follows:

Figs. 3A – 3B are cross-sectional diagrams of a planarization process using anisotropic wet etching according to another preferred embodiment of ~~this~~ the present invention. In Fig. 3A, conductive lines 310a, 310b and 310c are on substrate 300, and conductive lines 310a, 310b and 310c can be, for example, gates or metal lines. An insulating layer 320 is then formed on the conductive lines 310a, 310b and 310c and the substrate 300.

PAGE 7/14 * RCVD AT 4/28/2004 10:13:02 AM [Eastern Daylight Time] * SVR:USPTO-EFXRF-1/4 * DNIS:8729306 * CSID:248 433 7274 * DURATION (mm-ss):03-50

Please amend the paragraph beginning at page 5, line 19 as follows:

The distance between conductive lines 310a and 310b is larger, i.e., the pattern density is lower in this area. The distance between conductive lines 310b and 310c is shorter, i.e., the pattern density is higher in this area. Therefore, the etching solution slows by the area between conductive lines 310a and 310b at a higher flow rate and flows by the area between conductive lines 310b and 310c at a lower flow rate. That is, the etching rate is higher in the area between conductive lines 310a and 310b and is lower in the area between conductive lines 310b and 310c. Therefore, although the levels of the area between conductive lines 310a and 310b and the area between conductive lines 310b and 310c are the same, the etching rate is different. This problem can be solved by a dummy pattern.

Please amend the paragraph beginning at page 6, line 1 as follows:

The method of forming a dummy pattern comprises forming an insulating layer 330 on the insulating layer 320 in Fig. 3A. The material of the insulating layer 330 is preferred to be the same as that of the insulating layer 320, and the thickness of the insulating layer 320 is about the same as the level difference between the top surface and the bottom surface of the insulating layer 320. In Fig. 3B, a dummy pattern 330a is formed after photolithography and etching. Therefore, the pattern density of the area between the conductive lines 310a and 310b is about the same as the area around the conductive lines 310b and 310c, and thus the etching rate can be almost the same in these two areas. The steps ~~are~~ to be performed ~~is~~ are similar in the description of Fig. 3B, therefore ~~it is~~ they are omitted here.

PAGE 8/14 * RCVD AT 4/28/2004 10:13:02 AM [Eastern Daylight Time] * SVR:USPTO-EFXRF-1/4 * DNIS:8729306 * CSID:248 433 7274 * DURATION (mm-ss):03-50

Please amend the paragraph beginning at page 6, line 12 as follows:

From the embodiments described above, this invention can use a single step to planarize a rugged surface to increase its planarity. Hence the CMP's drawbacks such as scratches and removing abrasive particles can be eliminated.

PAGE 9/14 * RCVD AT 4/28/2004 10:13:02 AM [Eastern Daylight Time] * SVR:USPTO-EFXRF-1/4 * DNIS:8729306 * CSID:248 433 7274 * DURATION (mm-ss):03-50